



Industrial Test of Integrated Circuits

Digital Test Training on V93K ATE



PART 1:

DATASHEET **ANALYSIS**

74ACT299 GENERAL DESCRIPTION

8-bit universal shift/storage register with tristate outputs.

Pin description

Pin Names	Description	
СР	Clock Pulse Input	S 0 —
DS ₀	Serial Data Input for Right Shift	\OE1
DS7	Serial Data Input for Left Shift	\OE2
S ₀ , S ₁	Mode Select Inputs	I/O4 —
MR	Asynchronous Master Reset	I/O2 —
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs	1/00 —
1/0 ₀ –1/0 ₇	Parallel Data Inputs or	Q0 —
	3-STATE Parallel Outputs	WR -
Q ₀ , Q ₇	Serial Outputs	GND -

Logic diagram



Truth table

	Inp	uts		Response
MR	S ₁	S ₀	СР	
L	Х	Х	Х	Asynchronous Reset; $Q_0 - Q_7 = LOW$
н	Н	н	~	Parallel Load; I/O $_n \rightarrow Q_n$
н	L	н	~	Shift Right; $DS_0 \rightarrow Q_0, Q_0 \rightarrow Q_1$, etc.
н	Н	L	~	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
н	L	L	х	Hold

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Four modes of operation controlled by (S_1, S_0)

20

19

18

17

16 15

14 - 1/03 I/O1

13

12 11

1 2

3

5 6

9

10

4ACT299

Vcc

S1

DS7

Q7

1/07

- 1/05

CP

DS0

- o hold (store)
- o shift left
- o shift right
- o load data
- Asynchronous reset controlled by \overline{MR} (active on low)

DC Electrical Characteristics (ACT)

Symbol	Paramotor	v _{cc}	T _A =	25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Unite	Conditions	
Symbol	Falameter	(V)	Тур	Gu	aranteed Limits	Onits	Conditions	
VIH	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$	
	Input Voltage	5.5	1.5	2.0	2.0	v	or $V_{CC} - 0.1V$	
VIL	Maximum LOW Level	3.0	1.5	0.8	0.8	N/	$V_{OUT} = 0.1V$	
	Input Voltage	4.5	1.5	0.8	0.8	v	or $V_{CC} - 0.1V$	
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	L 50 A	
		5.5	5.49	5.4	5.4	v	$100T = -50 \mu A$	
							$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		4.5	0.0001	3.86	3.76	V	I _{OH} = -24 mA	
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 5)	
V _{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	L _ 50 u A	
	Output Voltage	5.5	0.001	0.1	0.1	v	1 _{OUT} = 50 μA	
							$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		4.5		0.36	0.44	V	I _{OL} = 24 mA	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 5)	
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μΑ	$V_I = V_{CC}$, GND	
ICCT	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1V$	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 6)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μΑ	V _{IN} = V _{CC} or GND	
I _{OZT}	Maximum I/O						V_{I} (OE) = V_{IL} , V_{IH}	
	Leakage Current	5.5		±0.3	±3.0	μA	$V_I = V_{CC}, GND$	
							$V_0 = V_{CC}, GND$	

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions

Supply Voltage (V _{CC})	
(Unless Otherwise Specified) 'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (VI)	0V to V _{CC}
Output Voltage (V _O)	0V to V _{CC}
Operating Temperature (T _A) 74AC/ACT 54AC/ACT	-40°C to +85°C -55°C to +125°C
	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices	
V _{IN} from 0.8V to 2.0V V _{CC} @ 4.5V, 5.5V	125 mV/ns

	AC (Operating	Requireme	nts & Electrical	Characteristics	(ACT)
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		Vcc	T _A = -	+25°C	T _A = -40°C to +85°C	
Symbol	Parameter	(V)	C _L =	50 pF	C _L = 50 pF	Units
		(Note 10)	Тур	Guar	anteed Minimum	
te	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.5	ns
ц	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	-2.0	1.0	1.0	ns
t _s	Setup Time, HIGH or LOW I/O _n to CP	5.0	1.5	4.0	4.5	ns
ţн	Hold Time, HIGH or LOW I/On to CP	5.0	-1.0	1.0	1.0	ns
t _s	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	1.5	4.5	5.0	ns
tu	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	-1.0	1.0	1.0	ns
tw	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns
tw	MR Pulse Width, LOW	5.0	2.0	3.5	3.5	ns
teen	Recovery Time, MR to CP	5.0	0	1.5	1.5	ns

AC Operating Requirements for ACT

		Vcc		T _A = +25°C		T _A = -40°	C to +85°C	
Symbol	Parameter	(V)		$C_L = 50 \text{ pF}$		C _L =	50 pF	Units
		(Note 9)	Min	Тур	Max	Min	Мах	Í
f _{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t _{PLH}	Propagation Delay CP to I/On	5.0	4.5	8.5	12.5	4.5	13.5	ns
t _{PHL}	Propagation Delay CP to I/O _n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t _{PHL}	Propagation Delay \overline{MR} to Q_0 or Q_7	5.0	4.0	14.0	15.0	4.0	18.0	ns
t _{PHL}	Propagation Delay MR to I/On	5.0	4.0	13.0	14.5	3.5	17.5	ns
t _{PZH}	Output Enable Time OE to I/On	5.0	2.5	8.0	12.0	1.5	13.0	ns
t _{PZL}	Output Enable Time OE to I/On	5.0	2.0	8.0	12.0	1.5	13.5	ns
t _{PHZ}	Output Disable Time OE to I/On	5.0	2.0	8.5	12.5	2.0	13.5	ns
t _{PLZ}	Output Disable Time	5.0	2.5	8.0	11.5	2.0	12.5	ns

1. Exercise: 74ACT299 – Test patterns for functional test

Referring to the truth table, fill missing instructions in the right column and complete the test vector columns for each pin when necessary (remember that no empty entries are allowed).

М	СР	S0	S1	DS	DS	10	10	10	10	10	10	10	10	Q	Q	INSTRUCTIONS
R				0	7	0	1	2	3	4	5	6	7	0	7	
0	1	0	0	1	1	1	1	1	1	1	1	1	1	Х	Х	Reset
1	1	0	0	1	1	L	L	L	L	L	L	L	L	L	L	Hold
1	1	1	1	0	0	1	0	0	0	0	0	0	0	Н	L	// Load 1000000
1	1	1	0	0	0	L	Н	L	L	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	Н	L	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	Н	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	н	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	L	Н	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	L	L	Н	L	L	L	
1	1	1	0	0	0	L	Ц	L	L	L	L	L	Н	L	Н	
1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L	
1	1	0	1	0	1	L	L	L	L	L	L	L	Н	L	Н	Shift left 1
																Shift left 1
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
1	1	0	0	0	0	Н	Н	L	L	L	L	L	L	Н	L	Hold
																// Load 10101010
																Hold
																Shift right 0
																Hold
																Reset
1	1	1	1	0	0	1	1	1	1	1	1	1	1	Н	Н	// Load 11111111
1	1	0	0	0	0	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L	
1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L	

2. Exercise: 74ACT299 – Values for parametric tests

Referring to DC electrical characteristics, extract the value guaranteed in the datasheet for the following parameters. Indicate whether it is a minimum or a maximum guaranteed value.

Datasheet guaranteed value	Test Conditions: T=25°C and Vcc=4.5V	Min or Max?
Vil =		
Vih =		
Vol =	with iol=24mA	
Voh =	with ioh=-24mA	

Referring to AC operating requirements and electrical characteristics, extract the value guaranteed in the datasheet for the following parameters. Indicate whether it is a minimum or a maximum guaranteed value.

Datasheet guaranteed value	Test Conditions:	Min or Max?
	T=25°C and Vcc=5V	
Setup time I/O vs CP =		
Setup time DS0/DS7 vs CP =		
Setup time SO/S1 vs CP =		
Hold time I/O vs CP =		
Hold time DS0/DS7 vs CP =		
Hold time SO/S1 vs CP =		
Propagation delay I/O vs CP =		
Propagation delay Q0/Q7 vs CP =		



FIRST STEPS WITH SMARTEST: PART 1

Step 1: Launching SmarTest

1/ Open the VNC icon



Ask the teacher your login and refer to the following table to get your password, the VNC display number and the default machine M to use for offline connection.

Login trainXv93	Password #trainXv93#	Y: VNC display	M: Default machine for offline connection
		number	
train1v93	#train1v93#	71	verigyon2016
train2v93	#train2v93#	72	verigyon2016
train3v93	#train3v93#	73	verigyoff2017
train4v93	#train4v93#	74	verigyoff2017
train5v93	#train5v93#	75	verigyoff2017
train6v93	#train6v93#	76	verigyoff2017
train7v93	#train7v93#	77	verigyoff2017
train8v93	#train8v93#	78	verigyoff2017

2/ Use this information to fill the VNC Connect window: M.cnfm.fr:Y with **M** = verigyon2016 **OR** verigyoff2017



Once the connection established, according to the machine you connected, you should get one of the 2 following windows.



3/ From the start menu « S also called RedHat menu), the shortcuts to launch SmarTest[®] are located in the menu "Verigy" or "Advantest".

less Accessories	*	
ৰ Games	*	
🔖 Graphics	>	
Internet	"Online" mode	
💰 Office	, Online mode	
🧑 Preferences	available only on	
🥳 Programming	VerigvON	
🅼 Sound & Video	•	
🚚 System Settings	•	
😽 System Tools	•	
🍟 Verigy	• 🕎 SmarTest	
Control Center	SmarTest Online Documentation	
a Find Files	SmarTest offline	"Offline" mode
🗭 Help	🕰 hp93000	To be used
🙀 Home	🔀 kill SmarTest	lo be useu
👩 Run Command	🗾 kill hp93000	by default
🚱 Lock Screen	Switch Version	
💩 Logout "demo"		

When starting **SmarTest**[®], you will have displayed a window called Workspace Launcher window. Select Ok if you have the following path: */home/trainXv93/workspace_MONTPELLIER*; otherwise "Browse" through the directories to access it.

	V Workspace Launcher	
	Select a workspace	
	SmarTest Eclipse Workcenter stores your projects in a folder called a workspace.	
	Workspace: /home/train1v93/workspace_MONTPELLIER	<u>B</u> rowse
NEVER	SELECT	
THIS C	PTION	
	Use this as the default and do not ask again	
	ОК	Cancel

Never save your test program under this path. This is not the expected test program directory. It will induce errors.

When launching SmarTest[®], 3 windows appear on the screen:

• « **Operation Control** » window allows controlling tasks execution on tester.

Used to format datalog stream results.



« ui_report » window allows following the communication between the tester and SmarTest[®].
 It is very important to regularly look at this window to verify if any error or warning messages appear.

▼ui_report.ORG.PROD -	O X
<u>F</u> ile <u>O</u> ptions Help Mode Datalog	
Tester State DISCONNECTED (OFFLINE)	
Tester Operation NOT monitored (DISABLED)	
Dev_license_file: None, model file used for licensing INFO: (dataformatter) Starting dataformatter version 1,1,11 Nov 22 2007 20:47:41 INFO: (dataformatter) Log file /users/latorre/dataformatter.log initialized. INFO: (dataformatter) Using global config file: /etc/opt/hp93000/soc/datalog/formatter.s Loading will be done through import filter '/opt/hp93000/soc/com/lbin/hp83_import' Prior to save '/opt/hp93000/soc/com/lbin/hp83_presave' will be run	
Report Forwatter .default.PROD	2

M2-EEA

• « SmarTest Eclipse Workcenter » window where the users will find all tools to develop a test program.



Step 2: Creating SmarTest Device directory

From the tool bar of the "Smartest Eclipse Workcenter" window, select **93000/Device/New Device**; from the opened window, browse the path **/home/trainXv93/M2/** and enter the name **74ACT299** to create the new test program directory (refer to picture below).

<u>9</u> 3000 <u>Wi</u> ndow <u>H</u> elp	_	V New Device	o x				
<u>S</u> etup	> _v	Setup new device					
<u>R</u> esults	>	😣 No device path specified					
<u>D</u> ebug	>						
Memory Test	>	Change to new device after creation					
S <u>c</u> an	>	Device path: /home/train1v93/M2/74ACT299 Browse	2				
<u>A</u> nalog	>						
Production	>	Device technology: cmos	*				
S <u>y</u> stem	>	Licensing file: Licensing file cannot be selected at device creation	~				
<u>D</u> evice	Mew Device	V3 delay adjust Fast bidirectional capability					
UI updates suspended	e Change Device	entre entiere					
🖉 Connect			-				
X Disconnect		PPU tester model: act					
🖲 Break MCD		Device cycles: 256 Waveform sets: 16 Timing sets: 256					
		Level sets: 32 PDC sets: 1 DPS sets: 32					
		M sets: 32 Routing sets: 32 Testpoints: 0					
		RFI to RFE compatibility mode					

Return to the RedHad menu and open a "Terminal" window from "System Tools".

Type the following command to access to your device directory:

> cd /home/trainXv93/M2/74ACT299

> Is (to see all the sub-directories automatically created)

💙 Shell - Konso	le				:	×
Session Edit V	liew Bookmarks S	Settings Help				
1 1						
[train1v93@Ve	rigyOFF2 74ACT2	:99]\$ ls			•]
TestlvEthod analog_contro applicat bitmap bitmap_conf calibration ch_attributes configuration [train1v93@Ve	data_set di_report error_map fail_memory format levels license lock_file rigyOFF2 74ACT2	<pre>memt_llapg memt_patterns memt_repair pin_attributes profiles report routing scan 99]\$ ■</pre>	scan_res scrambling shmoo state_list testflow testflow_vee testfunc testprog	timing timing_dgrm vectors wafertyp waste waveform		
					2	

Reminder: Procedure to exit SmarTest and VNC

- Exiting SmarTest: click "File > Exit"
- Exiting VNC: click on the cross 🗵 (DO NOT LOGOUT!)

FIRST STEPS WITH SMARTEST: PART 2

Now, you are going to setup the basic elements: PINS, LEVELS, TIMING, PATTERN.

Step 1: PINS

Depending on the progress of the course, the pin configuration will be either created by the trainees or given by the trainer.

To copy an existing pin configuration file:

- OPEN a terminal window.
- Type the following command:
 - > cp /home/trainer/74ACT299/INIT_FILES/pins_103 /home/trainXv93/M2/74ACT299/configuration/.
- From the **Test Program Explorer** window on **SmarTest**, select the "**Pin Configuration**" grey item (grey means not loaded). From the right click menu, load this "Pin Configuration" file.

♥ 93000 Setup - SmarTest Eclipse Workc	enter - /home/train1v93/workspace_ALGODONE	- 8 X
<u>F</u> ile <u>E</u> dit <u>N</u> avigate Se <u>a</u> rch <u>P</u> roject	<u>9</u> 3000 <u>R</u> un <u>Wi</u> ndow <u>H</u> elp	
📑 🕶 📓 👜 🖬 🗛 - 🎉 - 📕 - 🖾 - 5	┇╸५╸ ៙╸ үँ ╸ ぬ╸ タ ि० ダ 🎗 🕒 🍭 இ - ৠ - १२ ०० ०	
F≎ ₩ 02000 Setur		
South Setup		
Test Program Explorer 🛛 Navigator		
/home/train1v93/ALGODONE/74ACT299		
	Select file to load	
Device Information		
S < Test Program>	New Folder Delete File Rename File	
Test Flow>	/home/train1v93/ALGODONE/74ACT299/configuration	
▶ 🐼 < Pin Configuration>	Folders A Files	
∠ <pre>∠</pre> Levels>		
Timing>		
<pre>Pattern></pre>		
Pin Attributes>		
🖉 <test control=""></test>		
🔆 <analog control=""></analog>		
A₂ <waveform></waveform>		
🐎 <routing></routing>	Selection: /home/train1v93/ALGODONE/74ACT299/configuration	
 User Procedure> 		• - D
🖇 <profile></profile>		
Testfloor Information	X <u>C</u> ancel	
Application Data>		
() <wafer></wafer>	INFO: createDefaultProfiles(): Created 'profiles' subdir of device for profile st	uppo:
Execution Input>	SmarTest WorkCenter Ready!	
		-
■ <data bridge=""></data>	v (///	>
□ □ ◆ Pin Configuration		

Have a look at the pins and pin groups setup:

93000 Setup - Pin Setting - SmarTest Eclip:	se Worl	kcenter – /hom	e/train1∨93/wo	rkspace_ST_R	OUSSET			_ @ X
<u>F</u> ile <u>E</u> dit <u>N</u> avigate Se <u>a</u> rch <u>P</u> roject <u>9</u> 30	<u>File Edit N</u> avigate Se <u>a</u> rch <u>P</u> roject <u>9</u> 3000 <u>R</u> un <u>Wi</u> ndow <u>H</u> elp							
➡ - 🔛 👜 🗟 🛝 - 発 - 🔳 - 🖾 - 岩 -	📬 🔛 📾 🖬 🗛 🎧 🗰 🖼 😤 🖏 📾 👘 🕴 🗸 🚱 🚱 🔗 🚱 🖉 🏷 🖉 🌾 🖗 🖉							
■ ¹ ¹ ¹ 93000 Setup		2						
	40 mi							
Hest Program Explorer 23 Navigator	l ⊗F Pin	Setting X						
/nome/train1v93/SI_ROUSSEI/74AC1299	Cito :	1 ^ 01	1					.
	Sile :	⊥ v Or		1	1			
▽ bevice Information		Pin No	Pin Name	Mode	Туре	DUT Board	Tester Channel	
🗟 <test program=""></test>					-			
Test Flow>	1	12	CP	std	1	0.0	10302	
▽ 🖗 pins	2	18	DS7	std		0.0	10308	
🔗 Pin Setting	3	11	DS0	std	1	0.0	10301	
🖒 🗁 Groups	4	19	51	std		0.0	10309	
Ports	5	1	SU	sta	1	0.0	10310	
Core Allocation	0	9	_MK	sta	-	0.0	10316	
PPS Channel Mode	/	1/	Q7	sta	0	0.0	10307	
🕨 🔁 Utility Purpose	8	16	Q0	sta	0	0.0	10315	
Levels>	10	4	1/07	std	io	0.0	10211	
Timing>	11	15	1/05	std	io	0.0	10305	
<pre>Pattern></pre>	12	5	1/04	std	io	0.0	10312	
Pin Attributes>	13	14	1/03	std	io	0.0	10304	
Ø <test control=""></test>	14	6	1/02	std	io	0.0	10313	
Analog Control>	15	13	1/01	std	io	0.0	10303	
- Waveform>	16	7	1/00	std	io	0.0	10314	
Kouting>	17		Vcc		DPS+	10.0	DPS11	
Oser Procedure>								
> Critilie>								
Application Data	4							•

Step 2: LEVELS

Repeat the operation for the levels:

- Copy an existing levels file to your device level directory with the command:
 - > cp /home/trainer/74ACT299/INIT_FILES/levels_74ACT299 /home/trainXv93/M2/74ACT299/levels/.
- Return to the Test Program Explorer and load the levels:
 - 1. From the Test Program Explorer, select "levels" item
 - 2. From the right click menu, select "Load"
 - 3. From the "Select File to Load" window, select "levels_74ACT299"
- Open the Level Setup window from the level item in the Test Program Explorer (« open » from the right-click menu or double-click). Displayed values are defaults values.

From the menu "**Select**" of the Level Setup window, choose "**Show I/O Eqn & Specs Results**" to display the levels that will be applied to the device as specified by Eqn#, Sps# and Lset#.



You can access to the list of existing Eqn#, Sps# and Lset# from the menu "Select->Select Specification..." and choose the one you want to display.

		X Select Specification	
Level Setup Select Edit Doc Fornat 1/0 p.cs DP5 pins DP5 poweroattage Shou I/0 Eqn. & Specs Results Shou FAST Eqn. & Specs Results Select Specification Edit Specifications Edit Equations ser_in i in 0.000	of 1 L ↓	Reg Exp Filter : Specifications :	Eqn Sps Description 1 1 no specs - Vcc=4.5V - relaxed levels 2 1 Vocnom - relaxed levels 2 2 Vocmin - relaxed levels 2 3 Vocmax - relaxed levels 2 4 Voc=5.5V - relaxed levels
io_in i 0.000 io_out o 2.100 ser_out o 2.100	4.500 2.400 o 2.400 o	Reg Exp Filter : Levels :	Set Description 1 no termination 2 with active load 8
			(select) (cancel)

To understand how these values have been programmed:

- Choose "Edit Equations" from the menu "Select" to open the Level Equation Set Editor; look at the defined EQNSETs and LEVELSETs.

/var/opt/hp93000/soc/tmp/93k.VsQyE0/edit_lvleqn	_ 🗆 🗙
File Edit Search Preferences Shell Macro Windows	<u>H</u> elp
PI	🛛 🖬 🖬 Rev 🗐 RegExp 🗐 Case
/var/opt/hp93000/soc/tmp/93k.VsQyEO/edit_Ivleqn 1398 bytes	L: C:
71 EQNSET 2 "with specs" 72 73 74 SPECS 75 VCC [V] #supply voltage 76 VIL [V] #low level input voltage 77 VIH [V] #high level input voltage 78 VOL [V] #low level output voltage 79 VOH [V] #high level output voltage 80 81 82 DPSPINS Vcc 83 vout=VCC 84 ilimit=1000 85 t ms =4	
86 offcurr=act 87 88 LEVELSET 1 "no termination" 89 90 PINS ctrl ser_in 91 vil =VIL 92 vih =VIH 93	
94 PINS ser_out 95 96 vol= VOL 97 voh = VOH 98 99 PINS io_pins 100 101 vil = VIL 102 vih = VIH 103 vol = VOL 104 voh = VOH	

Choose "Edit Specifications" from the menu "Select" to open the Spec Tool; look at the Spec Variables and their values for the different SpecSets.
 Use the menu "Select" of the Spec Tool to choose among the list of existing specifications



Exercise: 74ACT299 – Basic Elements - Levels

Using the tools/editors available in SmarTest, find the information to fill in the following table.

Eqn	Spec	Lset	supply	all	_in	all	out
#	#	#	DPS value	Drive	values	Compar	e values
				low	high	low	high
2	1	1					
2	2	1					
2	3	1					

Are these levels appropriate to implement functional tests? Justify your answer.

Step 3: TIMING

Repeat the operation for the timing:

- Copy an existing timing file to your device level directory with the command:
 - > cp /home/trainer/74ACT299/INIT_FILES/timing_74ACT299 /home/trainXv93/M2/74ACT299/timing/.
- Return to the Test Program Explorer and load the timing:
 - 1. From the Test Program Explorer, select "timing" item
 - 2. From the right click menu, select "Load"
 - 3. From the "Select File to Load" window, select "timing_74ACT299"
- Open the Timing Setup window from the timing item in the Test Program Explorer ("open" from the right-click menu or double-click).

X Timing Setup		_			
Select Edit Dev	CycEdit Check Doc Dis	play Format			standard
WFset# 1 of 1	Tset# 1 of 1			Df.DC: [oyo: 2
Waveform] Timing			
pin/group	DevCyc		i/o ^{cycle>}	0	1
CP	1*		i 1		
mode	0*		i 1		
ser_in	0*		i 1		
			1		
io_pins	0*	_	0		
ser_out	0*		0		
(→

Select "DISPLAY->DOUBLE" to enlarge the window.

Create an appropriate format to visualize the waveforms for the different types of pin:

- from the menu "Format", choose "new"
- define a format that contains CP, _MR, mode, ser_in, ser_out, io_pins
- **<u>unselect</u>** the box "show same device cycle for all pins"
- save your changes

✓ Timing Setup Select Edit Dev	CycEdit Check Doc Display Forma	t t			standard
Eqn# 1 Sps# 1	Tset# 1 of 2	Por	rt:@	Df.DC:	cyc: 2
Specification	gross_func_specs Equatio	n <u>grus_</u> f	💙 - Define forma	nt - ///////////////////////////////////	×
Wave Table 👔	gross_func_wtb Timing	20MHz	pinlist:	СР	format name standard
pin/group	DevCyc	i/o cycle>	Copy	DS7 DS0 I∠07	CP p (paste) _MR p mode g (delate)
CP	0	i 3		1/06 1/05 1/04 1/03	ser_un g ser_out g io_pins g set default
_MR	0	i 3 1		I/02 I/01	get format
mode	0	i 3 1	grouplist:	CPandMR DxAndQx	unselect
ser_in	0	i 3 1		all_out ctrl io_in	↓ Show same device cycle for all pins
ser_out	0	0		io_out io_pins mode	Show prev/next device cycle column Show free resource column Show waveform numbers
		i 2 1		<u>ser_11</u>	save cancel
io_pins	0	0		x	
ť					

The Timing Setup window now shows one waveform for each pin or pin group defined in the format, as specified by Eqn#, Sps# and Tset#. If it is not the case, choose "**Show Eqn & Spec Results**" from the menu "**Select**" and fill the device cycle name you want to display for each pin or pin group in the "DevCyc" column.

To see all the waveforms defined for a given pin or pin group, click on the name of a pin or pin group and choose "**One pin**" from the menu "**Select**". It will show you all the defined waveforms for the chosen pin or pin group.

To see again all pins or pin groups, choose again "format pins" from the menu "Select".

To see the values of edge location for a given pin or pin group, click on the name of a pin or pin group and choose "**Edge delay**" from the menu "**Select**". It will show you the value of defined edge delays for the chosen pin or pin group.

Note: You can access to the list of existing Eqn#, Sps# and Tset# from the menu "Select->Select Specification..." and choose the one you want to display.

To understand the waveforms displayed in the Timing Setup window:

- look at the waveform table ("edit wave tables" from the menu "Select")
- look at the definition of edges location ("edit equations" from the menu "Select")
- look at the values of the spec variables ("edit specifications" from the menu "Select")

Exercise: 74ACT299 – Basic Elements - Timing

Using the tools/editors available in SmarTest, find the information to fill in the following tables for Eqn #1, Spec #1, Tset #1.

	Activation time	End time
СР		
Mode		
Ser_in		
10		

	Capture time
Ser-out	
10	

Is this timing appropriate to implement functional tests? Justify your answer.

Step 4: PATTERN

Repeat the operation for the pattern:

- Copy an existing pattern file to your device level directory with the command:
 - > cp /home/trainer/74ACT299/INIT_FILES/ pattern_74ACT299 /home/trainXv93/M2/74ACT299/vectors/.
- Return to the Test Program Explorer and load the pattern:
 - 4. From the Test Program Explorer, select "pattern" item
 - 5. From the right click menu, select "Load"
 - 6. From the "Select File to Load" window, select "pattern_74ACT299"

From the Test Program Explorer, double-click on "pattern_74ACT299" to display the pattern list in **Test Pattern Explorer window**.

For this example, the pattern list only contains 3 patterns.

Double-click on the pattern called "**func1**" and look at the detail of this pattern in the **Pattern Editor** (you should recognize the pattern from the first exercise).

Signal			Т	Т	T -	<u> </u>	T	<u> </u>	—	<u> </u>	ГГ		6	1														
Signal																				F								
			0	S	S	18	S	12	S	S	S	12	12	C	C	0	0	S										
			12	9	9	밀	9	9	9	9	9	9	9	2	2	2	2	의										
			P d	S	S7	8	5	5	l	8	3	8	6	0	1	5	E	R										
			Ū	Ö	Ö	ž	ž	¥	¥	×	¥	×	¥	ō	0	Š	S	2										
X-Mode Ar	ea																											
Protocol																												
Vector#	Instruction	Comment																										
0		reset	1	1	1	1	1	1	1	1	1	1	1	х	х	0	0	0										
1		hold	1	1	1	L	L	L	L	L	L	L	L	L	L	0	0	1				-				_		
2		par load 100	. 1	0	0	1	0	0	0	0	0	0	0	х	х	1	1	1		=	1-	Pa	uu	eri	n I	Edi	το	r:
3		shift right	1	0	0	L	н	L	L	L	L	L	L	L	L	1	0	1				di	sp	la	V C	on	te	nt
4	_	shift right	1	0	0	L	L	н	L	L	L	L	L	L	L	1	0	1					c P					
5		shift right	1	0	0	L	L	L	н	L	L	L	L	L	L	1	0	1				0	r a	р	ati	ter	n	
6		shift right	1	0	0	L	L	L	L	н	L	L	L	L	L	1	0	1										
7		shift right	1	0	0	L	L	L	L	L	н	L	L	L	L	1	0	1										
8		shift right	1	0	0	L	L	L	L	L	L	н	L	L	L	1	0	1										
9		shift right	1	0	0	L	L	L	L	L	L	L	н	L	н	1	0	1										
10		shift right	1	0	0	L	L	L	L	L	L	L	L	L	L	1	0	1										
11	_	shift left	1	0	1	L	L	L	L	L	L	L	н	L	н	0	1	1										
12		shift left	1	0	1	L	L	L	L	L	L	н	н	L	н	0	1	1										
13	_	shift left	1	0	0	L	L	L	L	L	н	н	L	L	L	0	1	1										
14	_	shift left	1	0	0	L	L	L	L	н	н	L	L	L	L	0	1	1		Н								
15		shift left	1	0	0	L	L	L	н	н	L	L	L	L	L	0	1	1										
16	_	shift left	1	0	0	L	L	н	н	L	L	L	L	L	L	0	1	1										
17	_	shift left	1	0	0	L	н	н	L	L	L	L	L	L	L	0	1	1										
18	_	shift left	1	0	0	н	н	L	L	L	L	L	L	н	L	0	1	1										
19	_	hold	1	0	0	X	X	X	X	X	X	X	X	X	X	0	0	1										
20		par load 101	. 1	0	0	1	0	1	0	1	0	1	0	н	L	1	1	1										
21		hold	1	0	0	н	L	н	L	н	L	н	L	н	L	0	0	1										
22		shift left	1	0	0	L	н	L	н	L	н	L	L	L	L	0	1	1	_	Ŀ	J.							
<u>C</u>																			- 2	J								
Dattern Eve	lorer S2																											
me		Port	Tun		_	Т	Mo	mo	D (L v	Vav	οT	abl		_	_	_		Т	21/0	te et							
me		FUIL	yp	6			Me	no	n y		vav	en		6	_	_	_		14	ayt				_				
밝 func		0	Maii	n		١	ИV			g	ros	s_f	un	c_d	lev	cyd	_w	tb			1	Pa	att	er	n I	Ex	olo	re
19 func spe	ec search	0	Maii	n		4	SM			SI	peo	S	ear	ch	de	evc	vc	wtb				lis	st a		pa	att	err	IS

Reminder: Procedure to exit SmarTest and VNC

- Exiting SmarTest: click "File > Exit"
- Exiting VNC: click on the cross 🗵 (DO NOT LOGOUT!)



QUESTIONS ABOUT FIRST TEST CONCEPTS

Answer to the following questions relative to the test concepts.

Continuity test What is the purpose of this test?

What is the voltage applied on Vcc and device pins? Why?

The measured voltage on a given pin is 0.004V. What does it mean for this pin?

The measured voltage on a given pin is 2.0V. What does it mean for this pin?

Functional/Structural test

What are the voltages applied on inputs for low and high levels in case of a relaxed functional test?

What are the comparator threshold voltages typically used for interpretation of low and high levels in case of a relaxed functional test?

What are the main differences and similarities between structural and functional test approaches?



TEST PROGRAM DEVELOPMENT: FIRST TEST FLOW

Step 5: Create your first test flow

From the **Test Program Explorer** (Setup Perspective), select the "**Testflow**" item. To create a new test flow, perform the following actions:

- From the right click menu, select "New".
- Enter the testflow name "first_flow" and click "Finish".

Project Ex III Test Progr & /mnt/share/Training_FirstSession_	Right-click on testflow item & Select 'New'
▽ 쀁 Device Information	
📓 <test program=""></test>	
🚰 TrainingFlow 🥂	
▷ Ø pins_soc	Vew Testflow
🛆 levels	Create testflow
👗 timing	Enter testflow name
i;;;] all.binl	
🕿 <pin attributes=""></pin>	Name: FirstFlow
💋 <test control=""></test>	Lanation (marking and Train a Train
💥 <analog control=""></analog>	Location: [/mnt/share/ training_Hists
🍫 <waveform></waveform>	
🍣 <routing></routing>	C Enter name of
Cuser Procedure>	new testflow
🖇 <profile></profile>	
<pre>Test Table></pre>	
Channel Attributes>	
Testfloor Information	Click 'Finish'
👂 陷 Test Results	
	⑦ <u>Finish</u> Cancel

• From the right click menu on the Testflow item, select **"Open with > Flow Sequence Editor"**. An empty flow is opened in the flow sequence editor.



Step 6: Setup the context

The next step is to setup the context, i.e. to specify the pins, levels, timing and pattern that will be associated to this test flow. For this, perform the following actions:

- Right-click in an empty zone of the testflow window and select "Open > Setups Page".
- Fill-in your primary files in the corresponding setup entry (pins_103, levels_74ACT299, timing_74ACT299, pattern_first_flow).

Se FirstFlow	×							
Start	l d				F	irstFlow 🛛		- 0
tte						Setup	File	
Pale	R. Dum Calastad	ALL . T	r					
1	Run Selected	AIL+ I			1	Pin Configuration		
	E Run lestilow	Cui+i			2	Levels		
	Run	-			3	Timing		
	Open	•			4	Pattern		
	Go To	•	Variables Page	Ctrl+Alt+,	5	Pin Attributes		
	Insert	,	Flags Page	Ctrl+Alt+.	6	Channel Attributes		
	Insert Floating Test Suite	Ctrl+I	Setups Page	Ctrl+Alt+/	7	Analog Control		
	∘≮ Cut				8	Waveform		
	Copy				9	Routing		
	👔 Paste				10	Test Table		
	🗱 <u>D</u> elete					_		
	CC Group							
	Ungroup							
	Move							
	Collapse All							
	Expand All							
	Preferences				Test	: Suites Parameters T	ests Bins Variables Flags Setups Informa	ition

• Return to Test Program Explorer, select the "**Testflow**" item and select "Load All Setups" from the right click menu.

Step 7: Insert Testsuites

Now you have to insert a test block for each test you want to perform. For this first test flow, you have to implement **4 tests**:

- a continuity test
- a functional test @Vccmin
- a functional test @Vccnom
- a functional test @Vccmax

To insert a new Testsuite, perform the following actions:

- Choose the insertion point and select "Insert > run and branch" from the right click menu
- Fill in the required information and click **"Finish"**.

😽 FirstFi	low 🕱	😧 bon hondadhaach Nob Waad	
Select	Start	New "Run And Branch" Node S The Test Method field must not be empty.	
insertion point	 Right-click or Open Palett & Select 'Run and Branch' 	Test Suite Name continuity Comment Test Method	
Image: Select Image: Provide the select <		Timing Equation	
中rint 中Print to Datalog 小f/Then 中Repeat Loop 中While Loop		Level Set	
中 For Loop 中 Assign Value 率 Assign Level Value 率 Assign Timing Value		Bnish Cance	el

Details on the required information for continuity and functional test blocks are given herafter (choices for timing and pattern information are given but <u>you have to make the appropriate choices regarding</u> <u>level information for each test block</u> – *refer to Exercise: Basic Elements* – *Levels in STEP 2*).

Continuity test

TESTSUITE FIELDS	VALUE	
Testsuite name		Continuity
Test Method		select " dc_tml>DcTest>Continuity"
Timing Equation		1
Timing Spec Set		1
Timing Set		1
Level Equation		Choose the appropriate Level Equation
Level Spec		Choose the appropriate Level Spec
Level Set		Choose the appropriate Level Set
Pattern		"func1"

Functional test

TESTSUITE FIELDS	VALUE	
Testsuite name		Functional_Vccmin/nom/max
Test Method		select "ac_tml > AcTest > FunctionalTest"
Timing Equation		1
Timing Spec Set		1
Timing Set		1
Level Equation		Choose the appropriate Level Equation
Level Spec		Choose the appropriate Level Spec
Level Set		Choose the appropriate Level Set
Pattern		"func1"

Step 8: Insert Bins

You have now to insert a bad bin in the failing branch of each test block and a good bin at the end of the test flow according to the information given in the following table.

BIN TYPE	INSERTION POINT	SOFT BIN #	SOFT BIN NAME	HARD BIN #	HARD BIN NAME
BAD	CONTINUITY Failing Branch	2	FAILED CONTINUITY	2	CONTINUITY
BAD	FUNCTIONAL Vccmin Failing Branch	3	FAILED FUNCTIONAL Vccmin	3	FUNCTIONAL
BAD	FUNCTIONAL Vccnom Failing Branch	4	FAILED FUNCTIONAL Vccnom	3	FUNCTIONAL
BAD	FUNCTIONAL Vccmax Failing Branch	5	FAILED FUNCTIONAL Vccmax	3	FUNCTIONAL
GOOD	FUNCTIONAL Vccmax Passing Branch (end of test flow)	1	PASS	1	PASS

To insert a new Bin, perform the following actions:

- Choose the insertion point and select "Insert > Good/Bad Bin" from the right click menu.
- Fill in the required information and click "Finish".

Step 9: Define parameters and limits

You have to setup the test conditions and limits of your **continuity test block** according to the following information.

<u>Field</u>	Value	Comment
pin list	@	all pins
test current	-50	uA
pass volt min	200	mV
pass volt max	800	mV
settling time	4	ms
measurement mode	PPMUpar/ProgLoad	(your choice)
polarity	SPOL/BPOL	(your choice)
output	ReportUI	

Practically to setup the test conditions and limits of a Testsuite, perform the following actions:

- Double-click on the Testsuite in the Test Flow Editor; the Properties View opens.
- In the **Properties** widow, unfold **"Test Methods"** (see figure herafter)
 - Unfold "Parameters" and replace default values by yours.
 - Unfold "Limits" and replace default values by yours.

Caution: Do not write the units when entering values.

8.	my_first_flow ⊠	- 0	🔲 Prop	erties 🛿 🚦 Outline	V 🖻 🖶 🎽 🗖	. 🗆
•	Start		type fil	ter text		
Ð			Proper	ty	Value	
lett			⊽ Te	est Method	dc_tml.DcTest.Continuity	
Pa	Continuity 2			Parameters	@, -50[uA], 4[ms], ProgLoad, BPOL, ON, passVolt_mV, ReportUI	
Ш	Ĭ Ī			pinlist	0	н
	Eunctional Vccmin 3			testCurrent	-50[uA]	
	· · · · · · · · · · · · · · · · · · ·			settlingTime	4[ms]	
				measurementMod	ProgLoad	=
	Functional_Vccnom			polarity	BPOL	
	ĭ			prechargeToZeroV	ON	Н
	Functional Vccmax			testName	passVolt_mV	
	<u> </u>			output	ReportUI	
			∇	Limits		
	V				, 200 <= X <=800	
	ð			Test Number		
				Limit Value	200 <= · X <= · 800	
			⊽ Flag	S		•

Functional test block takes no test conditions and no test limits (except the pinlist), so you don't have to change the default values.

Step 10: Flag setting and test execution (offline)

The final step before test execution is to set flags for each Testsuite to specify which results will be displayed in the UI-Report window.

For this, go to the **Properties** view of each Testsuite, unfold "**Flags**" and activate the following options:

- Output on pass
- Output on fail
- Pass value
- Fail value
- Per pin on pass
- Per pin on fail

🗆 Properties 🕱 type filter text Property Value Test Number Test Level 0 Bypass Set pass Set fail Hold Hold on fail Output on pass \checkmark Output on fail \checkmark Pass value \checkmark Fail value \checkmark Per pin on pass \checkmark \checkmark Per pin on fail Force serial Log Mixed Signal Waveforr Fail per label

The tests are now ready to be executed. You have 2 options from the Testflow editor:

- 1. Select a Testsuite and choose **"Run Selected"** from the right click menu. Only this test block is executed.
- 2. Click on any zone of the test flow and choose **"Run Testflow"** from the right click menu. The complete test flow is executed.

Try both these options and look at the UI-Report window to make sure you have no syntax error and to visualize the displayed results. (Clear the Report window before each execution).

<u>Note</u>: In the offline mode, the Continuity test fails in PMU mode (while it passes in PL mode), because the simulator returns 0 value for the measured pin voltage. To execute the complete test flow despite this fail, activate the Flag "**Set Pass**" of the continuity test in the **Properties** window. You should obtain a Pass when running the complete test flow.

Your first test flow is now complete and ready to be verified online. For this, quit the simulator mode and connect online to the tester.

Do not forget to disable the Flag "Set Pass" of the continuity test before going to the online mode.

Step 11: Online test execution

NOTE: In case you developed your test flow on Verigyoff2017, due to compatibility issues you should first copy a similar test flow developed on Verigyon2016. To do so, type the following command in a Terminal:

> cp /home/trainer/74ACT299/INIT_FILES/first_flow_Verigyon2016 /home/trainXv93/M2/74ACT299/testflow/.

Ask the teacher the availability of the online license. If OK, connect to the online machine **verigyon2016** using VNC. Keep the same login and password (cf. page 7 to

remember your password and VNC display number).

Once the VNC window is opened (purple background), start the online license from the RedHad menu **Verigy >SmarTest**"



In the Test Program Explorer window, check that the test program path is yours (/home/trainXv93/M2/74ACT299). Otherwise, click **"93000 > Device > Change Device"** and select the path relative to your test program.

From the Test Program Explorer, load your test flow (first_flow) and all the primary files (pins_103, levels_74ACT299, timing_74ACT299, pattern_74ACT299).

Open your test flow in the Flow Sequence Editor and perform the following experiments:

- 1. Execute the complete test flow and verify you obtain a PASS.
- 2. Execute only the continuity test and look at the results in the UI-Report window. Return to the **Properties** window of the continuity test and change the "**Polarity**" in the "**Parameters**" section. Execute the test and look at the results in the UI-Report window. Return to the **Properties** window of the continuity test and change the "**MeasurementMode**" in the "**Parameters**" section. Execute the test and look at the results in the UI-Report window.
- 3. Select a functional test block and change the test pattern to "func2" in the Properties window. Execute only this functional test ("Run selected"). What is the test result? To understand the origin of the problem, open the test pattern "func2" in the Pattern Editor (double-click on "func2"). From the menu Pattern, select Expanded Mode. Run again the functional test and look at the results in Pattern Editor: failing vectors are highlighted in red.

Correct the values applied on the "mode" inputs (S0 and S1). Run again the functional test.



QUESTIONS ABOUT PARAMETRIC TESTS

Answer to the following questions relative to parametric tests.

Vil/Vih tests

What is the purpose of Vil/Vih test?

Observe the VIL/VIH measurements displayed in the table below.

PIN	VIL	VIH
DS7	1.500000 V	1.785000 V
S0	1.395000 V	1.825000 V
S1	1.455000 V	1.845000 V
_MR	1.435000 V	1.740000 V

According to the data sheet values, do you think these tests pass at $T^{\circ}=25C$? Justify your answer.

Vol/Voh tests

What is the purpose of Vol/Voh test?

Referring to the datasheet, how many Vol/Voh tests should be implemented to exhaustively verify all Vol/Voh specifications? List them.

Setup and hold time tests

Do you agree with both definitions?

- The setup time is the maximum amount of time the data input must be held steady before the activation of the clock.
- The hold time is the minimum amount of time that the data have to be present before the activation of the clock.

If not, provide the correct definition.

Look at setup time measurements displayed in the table below.

PIN	SETUP TIME
100	3.493000 ns
101	3.431000 ns
102	3.294000 ns
103	3.210000 ns
104	3.227000 ns
105	3.232000 ns
106	3.192000 ns
107	3.393000 ns

According to the datasheet values, do you think this test passes at T°=25C? Justify your answer.

Propagation delay tests

What is the purpose of the propagation delay test?

Do the following measurements meet the specifications?

PIN	Prop delay
Q7	9.701000 ns
Q0	10.535000 ns

IMPLEMENTATION OF PARAMETRIC TESTS on 74ACT299

In this lab, you will run a more thorough test flow that includes not only continuity and functional tests but also some DC and AC parametric tests. The structure of the test flow will be provided. The objective of the exercise is to define the test conditions and limits of the parametric tests according to the device datasheet and to evaluate the actual circuit performances.

Note: to know which test conditions and/or test limits you have to change in each test block, return to page 6 of this document and consult the values you have extracted from the data sheet

Step 1: Copy an existing test flow and its associated primary files (offline)

- Open a terminal window from the RedHat menu « Solution >> .
- Copy the test flow file called "full_flow_2Modify" to your "testflow" directory with the command:
 - > cp /home/trainer/74ACT299/INIT_FILES/full_flow_2Modify /home/trainXv93/M2/74ACT299/testflow/.
- Copy the pattern file associated with this test flow to your "vectors" directory with the command:
 - > cp /home/trainer/74ACT299/INIT_FILES/pattern_full_flow /home/trainXv93/M2/74ACT299/vectors/.

The levels and timing files used for this full_flow are the same than for the first_flow (levels_74ACT299, timing_74ACT299).

Step 2: Modify the existing test flow (offline)

- Load the test flow from the Test Program Explorer and open it in the graphical editor (Flow Sequence Editor).
- Load the primary files associated to this test flow ("Load all setups").

You have now to modify the test flow in order to specify the correct test conditions and limits for the DC and AC tests.

The modification of the values will be done in the **"test control"** window (yellow window) for each test block. The procedure is the following:

- Select the first test block you want to modify.
- In the Properties window, select **"Test Function > Parameters"** and press **F3**. This will open the "test control" window.
- Change the default values by the values you have extracted from the datasheet.
- Once the changes are done, close the "test control" window and move to the next test block in the test flow.

8.	est2Complete ន	- 0	🔲 Properties 😫 😫 Ou	tline			√ (∃ ⊞ ▽ □ □		
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e	Functional		Property	Value						
ett				VIL_VIH						
Pa	Functional_Vccmin		Comment			X Test Control				_ ×
	ľ <u> </u>					Edit Doc				
	Eurctional Vccnom		▷ Timing	1, 1, 1		Input Volta	ge			
			Level	2, 4, 1		Sensitivity				
			Analog		_ 7					
	Functional_Vccmax 5	=	Pattern	gross_func	3		Ban			
	ii		Context	DEFAULT		pin list	L <mark>87</mark>	, SU, SI, _MR		
	Β		Test Type	Т						
	DC tests			vil_vih_tf				low	high	
			Parameters	inp_volt_sensitivity;	DS7,S0,S	nass level	V	0.8	2.00	+
			▷ Flags			pass level	1	1 0.0	1 2.00	1
	Ĭ –		Site Control							
	🕀 VOL VOH				×	O serial				
						parallel				
	Please clie	ck "OK" a	fter you finish editing parameters in Test Control							
						output	VIL	/VIH (\$P)		
	Ĭ									
				OK						
	<u> </u>			OK						
	· _ · · · · · · · · · · · · · · · · · ·									
	AC tests								P	

Practically, you have to modify the following test blocks:

- 1 Vil/Vih test:

only Vil and Vih values matter.

- 1 Vol/Voh test:

Vol/Voh + Iol/Ioh values have to be considered. The test control block also asks low/high limits for PMU clamp voltage; enter 0V and 5V respectively.

- 3 setup time tests:
 - DS0/DS7 (ser_in) versus CP
 - IO[0:7] versus CP
 - SO/S1 (mode) versus CP

- 3 hold time tests:

- DS0/DS7 (ser_in) versus CP
- IO[0:7] versus CP
- S0/S1 (mode) versus CP
- 2 propagation delay tests:
 - Q0/Q7 (ser_out) versus CP
 - o IO[0:7] versus CP

Once you have modified all the test blocks, save the new test flow under the name **"full_flow"** (click right on the test flow item in the Test Program Explorer and select choose "**save as**").

Step 3: Run the test flow (offline)

Run the test flow offline to verify that you don't have **any syntax error**.

<u>Note</u>: In the offline mode, a Fail might be obtained at any of the parametric tests because the simulator returns dummy values, and the test flow stops at the Fail result. In order to verify the syntax of the entire test flow, you should permit the complete execution of the test flow.

For this, perform the following actions:

- Open the test flow in the "Flow Data Editor" (click right on the test flow item in the Test Program Explorer and select "Open with > Flow Data Editor").
- Choose the "Flags" tab at the bottom of the window.
- Search the "**Global Overon**" flag and change its value it to "**on**". This will enable to continue the execution of the test flow until the final bin, even after reaching a "Bad" bin.

			>	ormation
			Ctrl+N	w
			F3	en
		OFlow Sequence Editor	•	en Wit <u>h</u>
	Flow Data Editor window	Flow Data Editor	10w To Merge	en Testf
		0	oject Explorer	ow in Pro
- 6		C_testflow 🛛	C_AC_testflow (DC_AC	😽 DO
- I I	Value	Flag Type	Flags	
	0	TESTFLOW	set_bypass_level	22
	off	TESTFLOW	hold_on_fail	23
	on	TESTFLOW	optimized_mode	24
	off	TESTFLOW	global_hold	25
	0 (Debug off)	TESTFLOW	debug_mode	26
	off	TESTFLOW	debug_analog	27
-	on	TESTFLOW	parallel_mode	28
	auto(on)	TESTFLOW	site_match_mode	29
	on	TESTFLOW	global_overon	30
	on	TESTFLOW	limits_enable	31
	on	TESTFLOW	test_number_enable	32
	1	TESTFLOW	test_number_inc	33
	1000000	TESTFLOW	test_num_col_offset	34
		TECTELONI	test number manager	25
	off	TESTFLOW	cesc_namer_namager	55
	off O	TESTFLOW	log_cycles_before	36

Return to the **Flow Sequence Editor** and run again the entire test flow. All test blocks are now executed, i.e. they all have a Pass or Fail result (as indicated by the green/red color of each test block).

Look at the results in the **UI-report** window. You should have two sections, the bottom section with the global Pass/Fail result and the top section with the detailed results for each test block. Separator between the 2 sections can be moved from the small square on the right side.

🗙 ui_report.ORG.PROD 📃 🗖	
<u>F</u> ile <u>Options</u> Help Mode Datalog	
Tester State DISCONNECTED (OFFLINE)	
Tester Operation NOT monitored (DISABLED)	
VIL_VIH inp_volt_sensitivity FAIL 135,000000 mV 4420,000000 mV 110,000000 Test_number: 6 Begin_limit_data; SPRN 101.1,02001.202001	
SSG: "DC.tests" Top Section: Top Section: Top Section: Sensitivity; all_in; V;0.8;2.0;0;VIL/VIH (\$P); End_limit_data Top Section: Detailed for each f	tion: l results test block
CP P 3375,000000 mV P 110,000000 mV DS0 P 4150,000000 mV F 2180,000000 mV DS7 P 4300,000000 mV F 2180,000000 mV I/00 P 2565,000000 mV P 975,00000 mV I/01 P 1240,000000 mV P 975,00000 mV I/02 P 3185,000000 mV P 725,00000 mV I/03 P 2105,000000 mV P 735,00000 mV I/03 P 3255,000000 mV P 735,000000 mV I/04 F 135,000000 mV P 2355,000000 mV I/05 P 1145,000000 mV P 2315,000000 mV S0 P 2355,000000 mV F 2435,000000 mV S1 P 4420,000000 mV P 565,000000 mV T S1 P 4420,000000 mV P 565,000000	ata
	 Separator
Device test FAILEDI Herrice test FAILEDI Herrice test FAILEDI Herrice test FAILEDI Global P Global P	Section: ass/Fail result
Report Forwatterdefault_PROD	

If you don't have the top section, perform the following actions:

- Open the test flow in the "Flow Data Editor" (click right on the test flow item in the Test Program Explorer, select "Open with > Flow Data Editor") and choose the "Flags" tab.
- Make sure that the flags "datalog_to_report_win", and "datalog_formatter" and "log_event_enable" are set to "on".
- Make sure that the flags "datalog_to_report_win", and "datalog_formatter" and "log_event_enable" are set to "on".

	Ela era	Elen Turc	Makia	
	Flags	Flag Туре	Value	
1	report to file	SYSTEM	on	
2	report to printer	SYSTEM	off	
3	datalog_to_file	SYSTEM	on	
4	datalog_to_printer	SYSTEM	off	
5	datalog_to_report_win	SYSTEM	on	
6	datalog_formatter	SYSTEM		
7	datalog_sample_size	SYSTEM	1	
8	graphic_result_display	SYSTEM	on	
9	state_display	SYSTEM	off	
10	print_wafermap	SYSTEM	off	
11	ink_wafer	SYSTEM	off	
12	max_reprobes	SYSTEM	1	
13	temp_monitor	SYSTEM	on	
14	calib_age_monitor	SYSTEM	on	
15	diag_monitor	SYSTEM	on	
16	current_monitor	SYSTEM	on	
17	log_events_enable	SYSTEM	On	
18	stdf_generation	SYSTEM	on	
19	tm_crash_as_fatal	SYSTEM	off	

• Return to the **Flow Sequence Editor** and run again the entire test flow. You should now have the two sections.

M2-EEA

<u>Note</u>: The default format used to display the detailed results in the UI-report window is a raw format that does not help to data readability.

To improve data readability, you can specify the use of a formatter with the following actions:

• Go to the "Operation Control" window. Click on "Production Settings", then click on "Report Formatter", choose "EventFormatter" and finish with "Select".



Go to the "UI-report" window. In the "Datalog" menu, choose "Enable Event Formatter". Then choose "Open Report Dialog". For each test type (except the analog one), select "Passed Pins", "Failed Pins" and "Limits" (when available). Click on "Set Testsuite Flags" and finish with "Close".

🗙 ui_report.ORG.PROD					
File Options Help Datalog Log File					
Enable Event Formatter					
Tester State	X Report Dialog				
Tester Operation NO ⁻ Load Formatter settings	Test Types FFV				
Clear Bins ******* production repo Started at: 2022052 Testflow execution device : 7 BUL_path : 7 testflow : D userprocedure : ******* begin testflow report data : ****** Device test PASSED! ******* 0000 0 0 0000 00000 00000 00000 00000 0000	Functional Test Parametric Test Hando Test TestHethod Output Testsuites that Output as Result Output as Result PArss FAIL PArss FAIL PArss FAIL Output as Result Output as Result Output as Result Output as Result Parsed Pins Failed Pins Failed Pins Failed Pins Failed Pins Failed Pins FFV Data Limits Limits Limits Haveforms)at			
****** 6 6 6 66666 66666 ****** ****** 6 6 6 6	Close Set Testsuite Flags 4 User Procedures				
BIN : 1 (PRSS) Ended at: 20220525 174121 ******* end testflow report data ****** INFO: (dataformatter) Completed Detailed STDF file per Lot: /home/azais/stdf/manual/main_Lot_1_May. I Report Formatter EventFormatter					

• Return to the **Flow Sequence Editor** and run again the entire test flow. Look at the detailed results in the top section of the **UI_report** window. The data are now much easier to read...

X ui_report.ORG.PROD	
File Options Help Datalog Log File	
Tester State DISCONNECTED (OFFLINE)	
Tester Operation NOT monitored (DISABLED)	
Input Voltage Sensitivity High; FAILED Pass/Fail Limit: 2.000000 V (Less or equal means passed) Measured Range: [0.300000 V 4.365000 V]	-
CP FAILED 2,435000 V	Top Section:
IST PASSED 0.310000 V I/D0 PASSED 1.035000 V	for each test block
1/01 FAILED 4.250000 V 1/02 FAILED 3.745000 V 1/03 PAISED 1.120000 V	formatted data
1/04 PASSED 0.30000 V 1/05 FAILED 4.365000 V 1/05 FAILED 4.365000 V	
1/07 PASED 0.985000 V S0 FAILED 3.155000 V	-
S1 PASSED 1.880000 V _MR PASSED 0.790000 V	
======= Ended Testsuite VIL VIH ===================================	
	O
Device test FAILED!	
****** 66666 66666 6 6 ***** ****** 6 6 6 6	Bottom Section: Global Pass/Fail result
****** 6 6 6 6 66666 ***** ****** 6 6 6 6	
BIN : 6 (FAIL VIL_VIH) Ended at: 20200719 103759	
	7
	12
Report Formatter EventFormatter	

Once all these steps are accomplished and everything is ok, your testflow is ready to be executed online. Quit the offline license. Do not forget to disable the Flag "Global Overon" in the Flow Data Editor before going to the online mode.

Step 4: Run the test flow (online)

- Connect to verigyon2016 and launch the online license.
- Load your test flow, open it in the graphical editor and load the primary files associated to this test flow ("Load all setups").
- Execute the test flow.
- Look at the global Pass/Fail result in the bottom part of the **UI-report** window. You should obtain a Pass!
- Look at the detailed results in the top part of the **UI-report** window. If data are not correctly formatted, repeat the procedure described in the preceding page to specify the use of a formatter and run again the entire test flow.
- Save the detailed results given in the top section of **UI-report** window in a text file (click in the top section and then click on menu "File > Save") and **quit the online license**.

Exercise: 74ACT299 – AC_DC_testflow – Test Results

From the analysis of the detailed results saved in the text file, write in the following table the **worstcase values** observed over the tested pins for each measurement. Evaluate the corresponding margin based on the datasheet information.

Measurement	Worst-case value	Datasheet guaranteed value	Margin (%)
VIL			
VIH			
VOL			
VOH			
Setup time Ser_in to CP			
Setup time IOx to CP			
Setup time Mode to CP			
Hold time Ser_in to CP			
Hold time IOx to CP			
Hold time Mode to CP			
Propagation delay CP to Ser_out			
Propagation delay CP to IOx			

 $Margin (\%) = \frac{(Measured Value \pm DS Limit)}{DS Limit} * 100$

Looking at these results, what can you say about the device?